CLAIM AMENDMENT

Please **CANCEL** claims 1-7, as follows.

1-7. (Cancelled)

8. (Original) A liquid crystal display, comprising:

a first substrate having a first insulating substrate and a pixel electrode formed on the first insulating substrate with a first opening pattern, the pixel electrode having upper and lower half regions, the first opening pattern having a first opening portion vertically partitioning the upper half region of the pixel electrode, and a second opening portion horizontally partitioning the lower half region of the pixel electrode;

a second substrate having a second insulating substrate facing the first insulating substrate and a common electrode formed on the second insulating substrate with a second opening pattern, the second opening pattern having a third opening portion proceeding in the vertical direction, and a fourth opening portion proceeding in the horizontal direction below the third opening portion, the first and the third opening portions being arranged in an alternate manner while vertically partitioning the upper half region of the pixel electrode into a plurality of micro-regions, the second and the fourth opening portions being arranged in an alternate manner while horizontally partitioning the lower half region of the pixel electrode into a plurality of micro-regions;

a liquid crystal material injected between the first and the second substrates; and

a spacer for maintaining the distance between the first and the second substrates.

9. (Original) A color filter substrate for a liquid crystal display, comprising:

an insulating substrate;

a black matrix formed on the insulating substrate;

a color filter formed at the black matrix;

a common electrode formed on the entire surface of the common electrode; and

first and second protrusions formed on the common electrode, the first protrusion having a first thickness, the second protrusion having a second thickness, the second thickness being greater than the first thickness.

10. (Original) The liquid crystal display of claim 9, wherein the first and the second protrusions are formed with one or more of a photosensitive organic insulating layer, a photoresist film, and a silicon-based insulating layer.

11. (Original) The liquid crystal display of claim 9, wherein the common electrode is formed of indium tin oxide or indium zinc oxide.

12. (Original) A method for fabricating a color filter substrate for a liquid crystal display, comprising the steps of:

forming a black matrix on an insulating substrate;

forming a color filter on the black matrix;

forming a common electrode on an entire surface of the insulating substrate;

depositing an insulating layer onto the common electrode; and

patterning the insulating layer to thereby form a first protrusion with a first thickness, and a second protrusion with a second thickness, the second thickness being greater than the first thickness.

13. (Original) The method of claim 12, wherein the insulating layer is formed with one or more of a photosensitive organic insulating layer, a photoresist film, and a silicon-based insulating layer.

14. (Original) The method of claim 12, wherein the common electrode is formed of indium tin oxide or indium zinc oxide.

15. (Original) The method of claim 12, wherein the first and the second protrusions are formed through a mask with a slit pattern corresponding to the first protrusion, and a transparent pattern corresponding to the second protrusion.

16. (Original) The method of claim 15, wherein the insulating layer is formed with a negative photosensitive organic insulating material.

17. (Original) The method of claim 12, wherein the first and the second protrusions are formed through a mask with a semitransparent pattern corresponding to the first protrusion, and an opaque pattern corresponding to the second protrusion.

18. (Original) The method of claim 17, wherein the insulating layer is formed with a positive photosensitive organic insulating material.

19. (Original) The method of claim 12, further comprising the step of forming a photoresist pattern differentiated in thickness on the insulating layer through one photolithography process.

20. (Original) A method for fabricating a liquid crystal display, comprising the steps of:

forming a thin film transistor array substrate such that the thin film transistor array substrate has a pixel electrode with a wiring line pattern, a switching circuit and an opening pattern;

forming a color filter substrate such that the color filter substrate has a common electrode, a color filter, a high molecular pillar, and a protrusion pattern;

combining the thin film transistor array substrate with the color filter substrate; and

injecting a liquid crystal material between the thin film transistor away substrate and the color filter substrate.

21. (Original) A method for fabricating a color filter substrate for a liquid crystal display, comprising the steps of:

forming a black matrix and a color filter on a transparent substrate in a sequential manner;

forming an over-coat layer on the color filter substrate;

forming a common electrode on the over-coat layer with a transparent conductive material;

coating a photosensitive resin onto the common electrode; and

exposing the photosensitive resin to light through a mask, and developing the light-exposed photosensitive resin to thereby fom1 a protrusion and a polymer pillar of different height, the mask having a first pattern with an opening width smaller than the resolution of the light exposing device, and a second pattern with an opening width larger than the resolution of the light exposing device.

22. (Original) The method of claim 21, wherein the protrusion has a width of 4-14 μm, and the polymer pillar has a width of 15-45 μm.

23. (Original) The method of claim 21, wherein the protrusion has a height of 1.0-1.2 μm, and the polymer pillar has a height of 3.0-4.5 μm.

24. (Original) The method of claim 21, further comprising the steps of hard baking the protrusion and the polymer pillar at a predetermined temperature such that the protrusion and the polymer pillar bear a predetermined strength, the height of the protrusion and the polymer pillar being controlled through varying the hard baking temperature.

25. (Original) The method of claim 24 wherein the hard backing temperature is in the range of 200-240° C.

26. (Original) A thin film transistor array substrate, comprising:

a gate line assembly comprising a gate electrode and a gate line;

a data line assembly comprising a data line crossing over the gate line, a source electrode, and a drain electrode;

a semiconductor pattern contacting the source and the drain electrodes while forming a thin film transistor together with the gate electrode, the source electrode, and the drain electrode;

an organic insulating pattern formed on the semiconductor pattern, the organic insulating pattern having a protrusion pattern with a first thickness, a contact hole exposing the drain electrode, and a flat portion with a second thickness; and

a pixel electrode formed on the organic insulating pattern while being connected to the drain electrode through the contact hole.

27. (Original) The thin film transistor array substrate of claim 26, wherein the semiconductor pattern is formed with hydrogenated amorphous silicon.

28. (Original) The thin film transistor array substrate of claim 26, wherein the semiconductor pattern has the same shape as the data line assembly except that the semiconductor pattern further has a channel region between the source and the drain electrodes.

29. (Original) The thin film transistor array substrate of claim 26. wherein the semiconductor pattern is formed over the gate electrode with an island shape.

30. (Original) A method for fabricating a thin film transistor array substrate, comprising the steps of:

forming a gate line assembly on a substrate, the gate line assembly comprising a gate line and a gate electrode;

forming a gate insulating layer on the substrate such that the gate insulating layer covers the gate line assembly;

forming a semiconductor pattern on the gate insulating layer;

forming a data line assembly on the gate insulating layer and the semiconductor pattern, the data line assembly comprising a data line, a source electrode, and a drain electrode;

forming an organic insulating pattern on the semiconductor pattern such that the organic insulating pattern has a protrusion pattern with a first thickness, a contact hole exposing the drain electrode, and a flat portion with a second thickness; and

forming a pixel electrode on the organic insulating pattern such that the pixel electrode is connected to the drain electrode through the contact hole.

31. (Original) The method of claim 30, wherein the formation of the organic insulating pattern is made through the steps of:

forming a photosensitive organic insulating layer on an entire surface of the substrate with the data line assembly;

exposing the photosensitive organic insulating layer in a selective manner such that the photosensitive organic insulating layer has a first portion blocked from light where the protrusion pattern is formed, a second portion entirely exposed to light where the contact hole is formed, and a third portion partially exposed to light; and

developing the selectively light-exposed organic insulating layer.

32. (Original) The method of claim 31, wherein the step of selectively exposing the organic insulating layer to light is made through a mask with a light blocking region placed over the first portion of the organic insulating layer, a light transmitting region placed over the second portion of the organic insulating layer, and a selectively light transmitting region placed over the third region while bearing a predetermined light transmission.

33. (Original) The method of claim 32, wherein a slit pattern or a semitransparent pattern is formed at the selectively light transmitting region of the mask.

34. (Original) The method of claim 31, wherein the step of selectively exposing the organic insulating layer to light is made through a first mask for exposing the second portion of the organic insulating layer to light, and a second mask for exposing the third portion of the organic insulating layer to light with a predetermined light transmission.

35. (Original) The method of claim 30, wherein the semiconductor pattern and the data line assembly are formed through photolithography based on a photoresist pattern of different in thickness.

36. (Original) The method of claim 35, wherein the photoresist pattern has a first portion placed over the data line assembly with a first thickness, and a second portion placed over the source and the drain electrodes with a second thickness smaller than the first thickness.

37. (Original) The method of claim 36, wherein the formation of the semiconductor pattern and the data line assembly is made through the steps of:

depositing a semiconductor layer and a conductive layer onto the gate insulating layer, and forming a photoresist pattern on the conductive layer;

etching the conductive layer using the photoresist pattern as a mask while partially exposing the semiconductor layer;

removing the exposed portion of the semiconductor layer and the second portion of the photoresist pattern through etching to thereby complete the semiconductor pattern while exposing the portion of the conductive layer between the source and the drain electrodes;

removing the exposed portion of the conductive layer to thereby complete the data line assembly; and

removing the first portion of the photoresist pattern.

38. (Original) The method of claim 35, wherein the photoresist pattern is formed through a mask with a first region with a predetermined light transmission, a second region with a light transmission lower than the first region, and a third region with a light transmission higher than the first region.